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ENERGY EFFICIENT CARRY SKIP ADDER USING SKIP LOGIC IN VARIOUS VOLTAGE LEVELS

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ABSTRACT

A carry skip adder (CSKA) structure has the high speed and very low power consumption. The speed of the structure is achieved by concatenation of all the blocks. The incrementation blocks are used to improve the efficiency of the carry skip adder structure. In existing method multiplexer logic is used, the proposed structure uses the AND-OR-Invert (AOI) and OR-AND-Invert (OAI) for the skip logic. The carry skip adder structure is realized with both fixed stage size and variable stage size where the delay is reduced, and speed is improved. A hybrid variable latency extension lowers the power consumption without affecting the speed of the circuit. The results are obtained using XILINX and it gives 42% and 37% improvements in the delay and energy of the structures. In addition to this structure, the power–delay product was low among all the structures, while having its energy–delay product was almost same as that of the conventional structure. Simulations on the proposed structure by using hybrid variable latency CSKA reduces the power consumption compared with the previous works and it produces a high speed.

KEYWORDS: Carry Skip Adder (CSKA), AOI, OAI, Energy Efficient, High Performance, Hybrid Variable Latency Adders